WHAT IS CLAIMED IS:

1. A computer structure, including processing elements and memory elements, the computer structure comprising:

a plurality of individual modules, each of said modules having said processing elements for processing data and at least one of said memory elements for storing data therein; and

an optical interconnect structure coupled to each of said plurality of modules for optically transporting data therebetween.

2. The computer structure of Claim 1, wherein said memory elements of said plurality of the modules form a shared memory.

3. The computer structure of Claim 2, wherein said memory elements on each of said plurality of modules comprises the highest level of the memory hierarchy.

4. The computer structure of Claim 1, wherein said processing elements include parallel processing elements.

5. The computer structure of Claim 1, wherein said optical interconnect structure includes a plurality of optical communication channels coupled to respective said modules to form an all-to-all interconnection therebetween.

6. The computer structure of Claim 5, wherein said optical communication channels include waveguide channels formed on a substrate.

7. The computer structure of Claim 6, wherein said waveguide channels extend and intersect in a single plane.

8. The computer structure of Claim 5, wherein said waveguide channels form a double plane waveguide and wherein at least one of said plurality of optical communication channels bends over at least another of said plurality of optical communication channels.

9. The computer structure of Claim 5, wherein said optical communication channels of said interconnect structure include optical fibers.

10. The computer structure of Claim 5, further comprising a plurality of optoelectronic components, each of said plurality of optoelectronic components being coupled between an end of at least one respective optical communication channel and a respective one of said plurality of modules.

11. The computer structure of Claim 10, wherein each of said plurality of optoelectronic components includes a light emitting diode coupled by an input thereof to an output port of said respective one of said plurality of modules for generating an optical signal corresponding to a digital signal output from said output port, said generated optical signal being optically coupled to a sending end of at least one respective optical communication channel for being transported therealong to an input port of at least one module of said plurality of the modules.

12. The computer structure of Claim 10, wherein each of said plurality of optoelectronic components includes a photodetector coupled by an input thereof to a receiving end of said at least one respective optical communication channel to receive an optical signal therefrom, said photodetector generating an electrical signal corresponding to said optical signal, said electrical signal being coupled to an input port of said respective module.

13. The computer structure of Claim 10, wherein said plurality of optoelectronic components reside on said optical interconnect structure.

14. The computer structure of Claim 10, further comprising storage elements associated with receiving and sending ends of said optical communication channels of said optical interconnect structure to temporarily store therein data.

15. The computer structure of Claim 5, wherein receiving ends of a portion of said plurality of optical communication channels are coupled to the same destination one of said plurality of modules, further comprising means at said destination module for conflict-free access of data to said destination module.

16. The computer structure of Claim 5, wherein receiving ends of at least two of said plurality of optical communication channels are coupled to the same one of said plurality of modules, further comprising broadcasting means associated with a sending end of each of said at least two optical communication channels for broadcasting the size of the data to be transmitted to said receiving ends, over each of said at least two optical communication channels, and

means associated with said receiving ends for issuing future time slots for data transmission on each of said at least two optical communication channels, and for sending said issued time slots to said sending ends of said at least two optical communication channels.

17. The computer structure of Claim 1, wherein the transport of the data in said optical interconnect structure is based on decentralized routing scheme.

18. The computer structure of Claim 1, wherein said optical interconnect structure is pipelined.

19. The computer structure of Claim 5, wherein the bending of each of said plurality of optical communication channels is limited by a predetermined radius of curvature.

20. The computer structure of Claim 5, wherein crossing angle of two of said plurality of optical communication channels is 90° or within a predetermined deviation from 90°.

21. The computer structure of Claim 5, wherein one optical communication channel bends over another optical communication channel, thus avoiding crossing thereof in a single plane.

22. The computer structure of Claim 5, wherein not more than two optical communication channels cross at the same crossing point.

23. The computer structure of Claim 22, wherein a distance between two crossing points is below a predetermined value.

24. The computer structure of Claim 22, wherein beyond said crossing point, a distance between two of said plurality of optical communication channels is below a predetermined spacing.

25. An interconnection fabric in a computer system for communication between a plurality of chips, wherein each chip includes processing elements and a memory element, said processing elements on said plurality of chips, in entirety thereof, forming the processing elements of the computer system, and said memory elements on said plurality of the chips, in entirety thereof, forming a shared memory in said computer system, the interconnect fabric comprising:

a plurality of optical communication channels, each coupled between respective two of said plurality of chips to form an all-to-all interconnection therebetween to transport data in optical form thereof between said respective chips.

26. The interconnection fabric of Claim 25, wherein said plurality of optical communication channels is formed as a plurality of waveguides fabricated on a substrate.

27. The interconnection fabric of Claim 26, wherein at least two of said plurality of said optical waveguides extend and intercross at a crossing point in a single plane on said substrate.

28. The interconnection fabric of Claim 25, wherein said shared memory comprises a first-level cache and wherein said processing elements form the processing elements of a parallel computer system.

29. The interconnection fabric of Claim 26, wherein at least one of said plurality of optical waveguide is bended.

30. The interconnection fabric of Claim 29, wherein the bending of said at least one optical waveguide is limited by a predetermined radius of curvature.

31. The interconnection fabric of Claim 26, wherein the crossing angle of said at least two optical waveguides at said crossing point is 90° or within a predetermined deviation from 90°.

32. The interconnection fabric of Claim 26, wherein at least one of said plurality of optical waveguides bends over at least another optical waveguide.

33. The interconnection fabric of Claim 26, wherein not more than two optical waveguides of said plurality thereof cross at the same crossing point.

34. The interconnection fabric of Claim 33, wherein a distance between two crossing points is above a predetermined value.

35. The interconnection fabric of Claim 33, wherein beyond said crossing point, a distance between said at least two optical waveguide is above a predetermined spacing.

36. An optical interconnect structure in a computer system including a plurality of processing elements for processing data and a plurality of memory elements for storing data, the optical interconnect structure comprising:

a plurality of optical communication channels, each channel having a sending end and a receiving end,

wherein a bending of each of said plurality of optical communication channels is limited by a predetermined radius of curvature;

wherein crossing angle of two of said plurality of optical communication channels crossing in the same plane is 90° or within a predetermined deviation from 90°;

wherein maximum two optical communication channels cross in a single crossing point,

wherein a distance between two crossing points is above a predetermined value, and

wherein beyond the crossing point, a distance between two of said plurality of optical communication channels is above a predetermined spacing.

37. The optical interconnect structure of Claim 36,

wherein in said computer system said processing elements include parallel processing elements, and said memory elements form the highest level of the memory hierarchy.

38. The optical interconnect structure of Claim 36, wherein said optical communication channels include waveguide channels formed on a substrate.

39. The optical interconnect structure of Claim 38, wherein said waveguide channels extend and intersect in a single plane.

40. The optical interconnect structure of Claim 38, wherein one of said waveguide channels bends over another of said waveguide channels.

41. The optical interconnect structure of Claim 36, further comprising a plurality of optoelectronic components, each optically coupled to said receiving end of a respective at least one of said plurality of optical communication channels, said optoelectronic components connecting data received at said receiving ends from optical to electrical form thereof for coupling to respective of said processing elements or to respective of said memory elements.

42. The optical interconnect structure of Claim 41, wherein each of said plurality of optoelectronic components includes a photodetector.

43. The optical interconnect structure of Claim 36, further comprising a plurality of optoelectronic components, each optically coupled to said sending end of a respective at least one of said plurality of optical communication channels, said optoelectronic components converting data received at said sending ends from respective of said processing elements or respective of said memory elements from electrical form into optical form thereof.

44. The optical interconnect structure of Claim 43, wherein each of said plurality of optoelectronic components includes a light emitting diode.

45. The optical interconnect structure of Claim 36, wherein the transport of the data is based on decentralized routing scheme.

46. The optical interconnect structure of Claim 36, wherein the transport of the data is based on pipeline scheme.

47. The optical interconnect structure of Claim 36, wherein said plurality of memory elements includes the highest level of the memory hierarchy, said plurality of the processing elements and said plurality of memory elements being distributed over a plurality of chips, respectively, and said optical communication channels being coupled between respective said chips to form all-to-all interconnection therebetween.

48. The optical interconnect structure of Claim 36, wherein processing of data is performed substantially in said processing elements.

49. The optical interconnect structure of Claim 36, further comprising storage means associated with said sending and receiving ends of said plurality of optical communication channels for temporarily storing data therein.

50. The optical interconnect structure of Claim 36, wherein at least a pair of said plurality of optical communication channels share a common receiving end or a common sending end.

51. A method for communicating data between processing elements of a processor and memory cells in a computer system, the method comprising the steps of:

distributing said processing elements and said memory cells on a plurality of chips,

interconnecting said plurality of chips by an optical interconnect structure, comprising a plurality of optical communication channels coupled between said chips to form an all-to-all interconnection therebetween,

outputting processed or stored data, in electrical form thereof, at an output port of at least one chip,

converting the data output at said output port of said at least one chip into optical form thereof,

transporting said data, in the optical form thereof, over at least one of said plurality of optical communication channels to at least another of said plurality of chips,

converting said transported data into electrical form, and

coupling said data, in electrical form thereof, to an input port of said at least another of said plurality of chips for processing or storing said data therein.

52. The method of Claim 51, further comprising the steps of:

transporting the data over said plurality of optical communication channels in a pipelined regime.

53. The method of Claim 51, further comprising the steps of:

intersecting at least two of said plurality of optical communication channels in a single plane.

54. The method of Claim 51, further comprising the steps of:

bending at least one of said plurality of optical communication channels over at least another of said plurality of optical communication channel, the bending being limited by a predetermined radius of curvature.

55. The method of Claim 51, further comprising the step of:

temporarily storing the transported data in a storage unit associated with a receiving end of said at least one optical communication channel prior to submitting said data at said input port of said at least another chip.

56. The method of Claim 51, further comprising the steps of:

broadcasting from a sending end of said at least one optical communication channel a size of data to be transported.

57. The method of Claim 56, further comprising the step of:

issuing time slots for said data transmission.

58. The method of Claim 51, further comprising the step of:

transporting the data over said plurality of optical communication channels in decentralized routing regime.